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(54) **SOLID-STATE IMAGE-PICKUP DEVICE AND DETECTION OF LIGHT SIGNAL THEREFROM**

(57) Abstract:
PROBLEM TO BE SOLVED: To provide a solid-state image-pickup device which can improve spectral sensitivity characteristics and conversion efficiencyand can offer superior linear photoelectric conversion characteristicsby reducing noise caused by surface capture or scattering of light-generated charge.
SOLUTION: Positive holes generated in a well region 15 by light illumination are guided to and embedded into a high-concentration buried layer 25which has an impurity concentration higher than that of the well region 15and which is embedded in the vicinity of a source diffused region 16 of an insulated gate type field effect transistor formed within the well region 15. The threshold of the transistor is changed by changing the quantity of the stored holes to detect a change in the threshold as the quantity of received light.

CLAIMS

[Claim(s)]
[Claim 1]A solid state image pickup device with which the

multiple arrays of the unit pixel provided with a euphotic diode and an insulated gate field effect transistor for lightwave signal detection were carried outcomprising:
A well area of one conductivity type formed in a semiconductor layer of an opposite conductivity type [diode / said / euphotic] on a semiconductor substrate of one conductivity type.
An opposite conductivity type drain diffusion region which has the opposite conductivity type impurity diffusion region formed in a surface of said well area and where said insulated gate field effect transistor was formed in a surface of said well area in one with said impurity diffusion region.
An opposite conductivity type source diffusion area which kept said drain diffusion region and an interval in a surface of said well areaand was formed in it.
A gate electrode formed via gate dielectric film on a well area between said drain diffusion region and said source diffusion area.
Channel regions where a current carrier of a surface of a well area under said gate electrode moves and which have an opposite conductivity type impurity layer.
A high concentration buried layer of one conductivity type which has impurity concentration higher than said well area near a source diffusion area in a well area under said channel regions.

[Claim 2]The solid state image pickup device according to claim 1wherein said high concentration buried layer is formed over the channel width direction whole region.
[Claim 3]The solid state image pickup device according to claim 1 or 2wherein the neighborhood of said source diffusion area is a partial area of the direction of channel length from said drain diffusion region to said source diffusion area and is said source diffusion area side.
[Claim 4]Said gate electrode has ring shape and said source diffusion area is formed in a surface of said well area of a center section of said gate electrodeThe solid state image pickup device according to any one of claims 1 to 3wherein said drain diffusion region is formed in a surface of said well area so that said gate electrode may be surroundedand said high concentration buried layer is formed in said well area so that said source diffusion area may be surrounded.
[Claim 5]The solid state image pickup device according to any one of claims 1 to 4wherein a gate electrode of said

insulated gate field effect transistor and its circumference are shaded.
[Claim 6]The solid state image pickup device according to any one of claims 1 to 5 connecting a load circuit to a source diffusion area of said insulated gate field effect transistorand constituting a source follower circuit.
[Claim 7]The solid state image pickup device according to claim 6wherein a source mode output of said source follower circuit is connected to video signal outputs.
[Claim 8]The solid state image pickup device according to any one of claims 1 to 7wherein said unit pixel is located in a line with a line writing direction and a line direction.
[Claim 9]A drain voltage supply line which both drain diffusion regions of an insulated gate field effect transistor of each of said unit pixel on a par with said line writing direction are connectedand sends drain voltage for said every lineA vertical-scanning-signals supply line which both gate electrodes of an insulated gate field effect transistor of each of said unit pixel on a par with said line writing direction are connectedand tells vertical scanning signals for said every lineTwo or more vertical output lines to which both source diffusion areas of an insulated gate field effect transistor of each of said unit pixel on a par with said line direction were connected and which were formed for said every sequenceA photodetection signal input terminal to which said each vertical output line was connectedrespectivelyand a photodetection signal output terminalA switch which has a horizontal scanning signal input terminal and was formed for said every sequenceA common level output line to which both photodetection signal output terminals of each of said switch were connectedA horizontal scanning signal supply line which tells a horizontal scanning signal which chooses one of said two or more vertical output lines to a horizontal scanning signal input terminal of said switchSaid drain voltage supply line is connected and said horizontal scanning signal supply line is connected with a drain voltage drive scanning circuit which supplies drain voltage selectively for every lineand a vertical-scanning-signals drive scanning circuit which said vertical-scanning-signals supply line is connectedand supplies vertical scanning signals selectively for every line. A horizontal scanning signal drive scanning circuit which supplies a horizontal scanning signal selectively for every sequenceA load circuit which forms a source follower among said one insulated gate field effect transistor which was

connected to said level output line and chosen by said drive scanning circuitThe solid state image pickup device according to claim 8 having the video signal outputs connected to a source mode output of said source follower. [Claim 10]The solid state image pickup device according to any one of claims 1 to 9wherein said solid state image pickup device is formed in said one semiconductor substrate. [Claim 11]. Were embedded near a n type source diffusion area of an insulated gate field effect transistor which formed this optical generating electron hole in said well area among an electron by which it was generated in a p type well area by optical exposureand an electron hole. A lightwave signal detecting method by a solid state image pickup device changing a threshold value of said insulated gate field effect transistor with quantity of an optical generating electron hole which drew and stored up in a p type high-concentration high concentration buried layer rather than said well areaand was this accumulatedand detecting variation of this threshold value as light income. [Claim 12]. Were embedded near a p type source diffusion area of an insulated gate field effect transistor which formed this optical generating electron in said well area among an electron by which it was generated in a n type well area by optical exposureand an electron hole. A lightwave signal detecting method by a solid state image pickup device changing a threshold value of said insulated gate field effect transistor with quantity of an optical generating electron which led and stored up in a n type high-concentration high concentration buried layer rather than said well areaand was this accumulatedand detecting variation of this threshold value as light income. [Claim 13]In a lightwave signal detecting method by the solid state image pickup device according to any one of claims 1 to 10Said semiconductor substratesaid well areaand said high concentration buried layer are p typesSaid semiconductor layersaid impurity diffusion regionsaid drain diffusion regionand said source diffusion area are n typesVoltage higher than operating voltage is impressed to said impurity diffusion regionsaid drain diffusion regionsaid gate electrodeand said source diffusion areaAn electron hole in said well area and said high concentration buried layer to said semiconductor substrate. A pixel is initialized by discharging an electronrespectively to said impurity diffusion regionsaid drain diffusion regionand said source diffusion areaand depletion-izing it to themAn electron hole and an electron are produced in a well area of said euphotic diode by optical exposureOperating voltage

is impressed to said impurity diffusion region and said drain diffusion regionAnd potential of a gate region of said insulated gate field effect transistor impresses voltage as for which a potential twist of said euphotic diode also becomes low to said gate electrodeMove inside of said well area for said optical generating electron holestore up said optical generating electron hole in said high concentration buried layerand operating voltage is impressed to said drain diffusion region and said gate electrodeWhile forming a reversal region of a low electric field in the direction of channel length on said high concentration buried layer which said optical generating electron hole accumulatedA high electric field field is formed in channel regions except said high concentration buried layer top in said direction of channel lengthOperating voltage that said insulated gate field effect transistor operates by saturation to said drain diffusion region and said gate electrode is impressedBy having formed said insulated gate field effect transistor in a source followerand having accumulated said optical generating electron hole in said high concentration buried layerchange of threshold voltage of said insulated gate field effect transistorA lightwave signal detecting method by a solid state image pickup device detecting a signal by changing into an electrical change of a source diffusion area of said insulated gate field effect transistor.

[Claim 14]In a lightwave signal detecting method by the solid state image pickup device according to any one of claims 1 to 10Said semiconductor substratesaid well areaand said high concentration buried layer are n typesSaid semiconductor layersaid impurity diffusion regionsaid drain diffusion regionand said source diffusion area are p typesLarger voltage to a negative side than operating voltage is impressed to said impurity diffusion regionsaid drain diffusion regionsaid gate electrodeand said source diffusion areaTo said semiconductor layeran electron hole for an electron in said well area and a high concentration buried layer Said impurity diffusion regionA pixel is initialized by discharging to said drain diffusion region and said source diffusion arearespectivelyand depletion-izing to themAn electron hole and an electron are produced in a well area of said euphotic diode by optical exposureOperating voltage is impressed to said impurity diffusion region and said drain diffusion regionAnd potential of a gate region of said insulated gate field effect transistor impresses voltage as for which a potential twist of said euphotic diode also becomes high to

said gate electrodeMove inside of said well area for said optical generating electronstore up said optical generating electron in said high concentration buried layerand operating voltage is impressed to said drain diffusion region and said gate electrodeWhile forming a reversal region of a low electric field on said high concentration buried layer which said optical generating electron accumulatedForm a high electric field field in channel regions except said high concentration buried layer topand operating voltage that said insulated gate field effect transistor operates by saturation to said drain diffusion region and said gate electrode is impressedChange of threshold voltage of said insulated gate field effect transistor by having formed said insulated gate field effect transistor in a source followerand said optical generating electron having been accumulated in said high concentration buried layerA lightwave signal detecting method by a solid state image pickup device detecting a signal by changing into an electrical change of a source diffusion area of said insulated gate field effect transistor.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to the lightwave signal detecting method by the MOS type solid state image pickup device and solid state image pickup device of a threshold voltage modulation method which are used for a video cameraan electronic cameraan image input cameraa scanneror a facsimile in more detail about the lightwave signal detecting method by the solid state image pickup device and a solid state image pickup device.

[0002]

[Description of the Prior Art]Since the semiconductor image sensor is excellent in mass production natureit is applied to almost all image input device equipment with progress of the miniaturized technology of a pattern. Especiallysince photosensitivity is high and the noise level is lowmany CCD (charge coupled device) to typical image devicessuch as a video camera and a facsimileis adopted.

[0003]Howeverthere are the following problems in CCD (charge coupled device)and development of the technology which can respond to these problems is desired. That issince ** power consumption and operating voltage need

complicated production technology unlike semiconductor devicessuch as high ** CMOS deviceand ** production technology with a high production cost differs from semiconductor devicessuch as a CMOS deviceit is hard making a complicated peripheral circuit in CCD.

[0004]In addition to such a situationthe application commercial scene of a solid state image pickup device is expandedand an MOS type solid state image pickup device is improved increasingly in recent years. It is becoming possible to create the device below a submicron by semiconductor miniaturization technology. On the other handabout the characteristic of the main part of an image sensorthe performance difference of an MOS type image sensor and CCD series was largeespeciallyin the MOS type image sensorthe improvement of a random noise characteristic and a fixed noise characteristic is neededand fundamental improved efficiency was desired.

[0005]on the other handthe amplifying circuit which can localize a photoelectric conversion part by progress of micro-lens technologyand consists of two to 3 transistor for every pixel by miniaturized technology can be accumulated nowand improvement in sensitivity was able to be aimed at. For this reasonit became possible to reduce in circuit the fixed pattern noise made with the thermal noise (kTC noise) generated in one MOS switch part among twoX and Yor element dispersion to some extent.

[0006]From such a pointwhat is called an active CMOS image sensor in which the detailed transistor amplifying circuits by a CMOS technology were formed in the pixel of a euphotic device attracts attention. Since an active CMOS image sensor does not need special production technology except the usual CMOS technologyit tends to integrate a CMOS peripheral circuit for the same chip as a euphotic portionand can manufacture it inexpensive. It has the feature that power consumption and operating voltage are small.

[0007]For this reasonit is expected very much towards realization of the one chip camera which carries a complicated digital disposal circuit in the future. The following examples are given as an advanced type of an active CMOS image sensor element. That isthe CMD (Charge Modulation Device: electric charge modulation element) mold solid state image pickup device is opened to JPS60-140752AJPS60-206063AJPH6-120473Aetc. This element is an element which adopted the CCD feature in optoelectric-transducer structureand in order to raise a numerical apertureit makes the gate electrode of the MOS transistor

photogate electrode structure. The electric charge generated by optical pumping is stored up in the gate oxide under the photogate electrode of a MOS transistorand the interface of a Si layerand current control is performed. Since **** of an electric charge is performed in a perfect depletion-ized modethe thermal noise characteristic of a transistor is improvable.

[0008]The BCMD (Bulk Charge Modulated Device) mold solid state image pickup device is opened to JPS64-14959A etc. As shown in drawing 13 (a)in order that this element might also raise a numerical aperturethe gate electrode 7 of the MOS transistor was made into photogate electrode structureand the accumulation layer 3 of the optical generating electric charge is formed on the N layer 2 under the photogate electrode 7. In this casethe accumulation layer 3 of the optical generating electric charge was established in the substrate 1 side rather than the channel regions of photogate electrode 7 directly underit controlled that the trap of the optical generating electric charge was carried out to the interface of the gate oxide 6 which touches the N layer 9 under the photogate electrode 7and the noise resulting from it is controlled. As for the mark 2as for N layer and 4a drain diffusion region and 8 are constant current power supplies a source diffusion area and 5 among drawing 13 (a).

[0009]The solid state image pickup device of the threshold voltage modulation method is opened to JPH2-304973A. In this elementit has ring gate electrode structure and a source diffusion area is formed in the center section of ring gate electrode structureand the drain diffusion region is formed so that a ring gate electrode may be surrounded. In this casethe drain diffusion region embedded and it serves as the high-concentration-impurities diffusion zone of a photo-diode. It is characterized by having provided the light sensing portion out of the transistor regionand providing a potential low place one place to a signal charge ranging from the source diffusion area to a drain diffusion region in the well area under some channel width fields of a channel width direction.

[0010]An embedding photo-diode is irradiatedan electric charge is generatedand a threshold value is controlled by this element by accumulation of the optical generating electric charge to an embedding photo-diode using a board bias effect. In particularit is the optical exposure of weak intensitywhen there are few optical generating electric chargesit is effectiveand an optical generating electric charge is brought together in a potential low

place to a signal chargethe unevenness of sensitivity is suppressedand control of fixed pattern noise is aimed at.
[0011]
[Problem to be solved by the invention]Howeverin a CMD type solid state image pickup devicesince the electric charge used for photoelectric conversion exists near a semiconductor surfacethe random noise component by electric charge capture or dispersion in the surface has the problem that it cannot remove. In a BCMD type solid state image pickup devicesince the charge storage layer 3 exists throughout the channel regions under the photogate electrode 7 as shown in drawing 13 (a)it will be difficult to fully saturate a transistorand as shown in drawing 13 (b)current/voltage characteristics will turn into a triode area property. For this reasonwhen transforming an optical generating electric charge into voltage by a source followerthere is a problem that sufficient linearity is not acquired.
[0012]Since carrier distribution in the charge storage layer 3 is scattered in the whole channel regions under the photogate electrode 7 and the whole channel regions contribute it to current abnormal conditionssince electric charge detecting capacity is also comparatively largethere is a problem that conversion efficiency is also inferiordeficiently in the linearity of potential abnormal conditions to the amount of injected charges. A CMD type and a BCMD type solid state image pickup device have a problem of degradation of a spectral sensitivity characteristic by multiple interference of incident light peculiar to an MOS structure of a light sensing portion in common by photogate electrode structure.
[0013]In photogate electrode structurethere is also a problem that a special and complicated manufacturing process -- formation of a photogate electrode which consists of a thin polysilicon film which has translucency is needed -- is required on a manufacturing process. a well under some channel width fields -- in a solid state image pickup device which provided a potential low place one place to a signal charge inside. Since it is in a well area under some channel width fields and the potential low place is provided ranging from a source diffusion area to a drain diffusion regionCurrent/voltage characteristics turn into the characteristic of a triode fieldand when transforming an optical generating electric charge into voltage by a source followerthere is a problem that sufficient linearity is not acquired.
[0014]The purpose of this invention is as follows.

Be made in view of an above-mentioned situationreduce noise resulting from surface capture or dispersion of an optical generating electric chargeand aim at improvement in a spectral sensitivity characteristic or conversion efficiency.
Provide a photodetection method by a solid state image pickup device and a solid state image pickup device which can acquire a photoelectric transfer characteristic excellent in linearityand can create a light sensing portion using the same production technology as production technology of CMOS.

[0015]
[Means for solving problem]In order that this invention may attain the above-mentioned purposeinvention of Claim 1 relates to a solid state image pickup deviceand is characterized by that the solid state image pickup device with which the multiple arrays of the unit pixel provided with the euphotic diode and the insulated gate field effect transistor for lightwave signal detection were carried out comprises the following.
The well area of one conductivity type formed in the semiconductor layer of the opposite conductivity type [diode / said / euphotic] on the semiconductor substrate of one conductivity type.
The opposite conductivity type drain diffusion region which has the opposite conductivity type impurity diffusion region formed in the surface of said well area and where said insulated gate field effect transistor was formed in the surface of said well area in one with said impurity diffusion region.
The opposite conductivity type source diffusion area which kept said drain diffusion region and the interval in the surface of said well areaand was formed in it.
The gate electrode formed via gate dielectric film on the well area between said drain diffusion region and said source diffusion areaThe high concentration buried layer of one conductivity type which has impurity concentration higher than said well area near the source diffusion area in the channel regions where the current carrier of the surface of the well area under said gate electrode movesand which have an opposite conductivity type impurity layerand the well area under said channel regions.

[0016]Invention of Claim 2 relates to the solid state image pickup device according to claim 1and said high concentration buried layer is characterized by being formed

over the channel width direction whole region. Invention of Claim 3 relates to the solid state image pickup device according to claim 1 or 2and the neighborhood of said source diffusion area is a partial area of the direction of channel length from said drain diffusion region to said source diffusion areaand is characterized by being said source diffusion area side.

[0017]Invention of Claim 4 relates to the solid state image pickup device according to any one of claims 1 to 3Said gate electrode has ring shape and said source diffusion area is formed in the surface of said well area of the center section of said gate electrodeIt is characterized by forming said drain diffusion region in the surface of said well area so that said gate electrode may be surroundedand forming said high concentration buried layer in said well area so that said source diffusion area may be surrounded.

[0018]Invention of Claim 5 relates to the solid state image pickup device according to any one of claims 1 to 4and it is characterized by shading the gate electrode of said insulated gate field effect transistorand its circumference. Invention of Claim 6 is characterized by starting the solid state image pickup device according to any one of claims 1 to 5connecting a load circuit to the source diffusion area of said insulated gate field effect transistorand constituting the source follower circuit.

[0019]Invention of Claim 7 relates to the solid state image pickup device according to claim 6and it is characterized by connecting the source mode output of said source follower circuit to video signal outputs. Invention of Claim 8 relates to the solid state image pickup device according to any one of claims 1 to 7and it is characterized by having located said unit pixel in a line with the line writing direction and the line direction. Invention of Claim 9 relates to the solid state image pickup device according to claim 8and both the drain diffusion regions of the insulated gate field effect transistor of each of said unit pixel on a par with said line writing direction are connectedThe drain voltage supply line which sends drain voltage for said every lineand the vertical-scanning-signals supply line which both the gate electrodes of the insulated gate field effect transistor of each of said unit pixel on a par with said line writing direction are connectedand tells vertical scanning signals for said every lineTwo or more vertical output lines to which both the source diffusion areas of the insulated gate field effect transistor of each of said unit pixel on a par with said line direction were connected

and which were formed for said every sequenceThe photodetection signal input terminal to which said each vertical output line was connectedrespectivelyand a photodetection signal output terminalThe switch which has a horizontal scanning signal input terminal and was formed for said every sequenceThe common level output line to which both the photodetection signal output terminals of each of said switch were connectedThe horizontal scanning signal supply line which tells the horizontal scanning signal which chooses one of said two or more vertical output lines to the horizontal scanning signal input terminal of said switchSaid drain voltage supply line is connected and said vertical-scanning-signals supply line is connected with the drain voltage drive scanning circuit which supplies drain voltage selectively for every lineThe vertical-scanning-signals drive scanning circuit which supplies vertical scanning signals selectively for every lineThe horizontal scanning signal drive scanning circuit which said horizontal scanning signal supply line is connectedand supplies a horizontal scanning signal selectively for every sequenceIt is connected to said level output lineand is characterized by having a load circuit which forms a source follower among said one insulated gate field effect transistor with said selected drive scanning circuitand the video signal outputs connected to the source mode output of said source follower.

[0020]Invention of Claim 10 relates to the solid state image pickup device according to any one of claims 1 to 9and it is characterized by forming said solid state image pickup device in said one semiconductor substrate. . Invention of Claim 11 related to the lightwave signal detecting method by a solid state image pickup deviceand were embedded near the n type source diffusion area of the insulated gate field effect transistor which formed this optical generating electron hole in said well area among the electron by which it was generated in the p type well area by optical exposureand the electron hole. The threshold value of said insulated gate field effect transistor is changed with the quantity of the optical generating electron hole which drew and stored up in the p type high-concentration high concentration buried layer rather than said well areaand was this accumulatedand it is characterized by detecting the variation of this threshold value as light income.

[0021]. Invention of Claim 12 related to the lightwave signal detecting method by a solid state image pickup deviceand were embedded near the p type source diffusion

area of the insulated gate field effect transistor which formed this optical generating electron in said well area among the electron by which it was generated in the n type well area by optical exposureand the electron hole. The threshold value of said insulated gate field effect transistor is changed with the quantity of the optical generating electron which led and stored up in the n type high-concentration high concentration buried layer rather than said well areaand was this accumulatedand it is characterized by detecting the variation of this threshold value as light income.

[0022]In the lightwave signal detecting method invention of Claim 13 relates to the lightwave signal detecting method by a solid state image pickup deviceand according to the solid state image pickup device according to any one of claims 1 to 10Said semiconductor substratesaid well areaand said high concentration buried layer are p typesSaid semiconductor layersaid impurity diffusion regionsaid drain diffusion regionand said source diffusion area are n typesVoltage higher than operating voltage is impressed to said impurity diffusion regionsaid drain diffusion regionsaid gate electrodeand said source diffusion areaTo said semiconductor substratean electron for the electron hole in said well area and a high concentration buried layer Said impurity diffusion regionA pixel is initialized by discharging to said drain diffusion region and said source diffusion arearespectivelyand depletion-izing to themAn electron hole and an electron are produced in the well area of said euphotic diode by optical exposureOperating voltage is impressed to said impurity diffusion region and said drain diffusion regionAnd the potential twist of said euphotic diode also impresses voltage which becomes low to said gate electrodethe potential of the gate region of said insulated gate field effect transistor moves the inside of said well area for said optical generating electron hole to itand said optical generating electron hole is stored up in said high concentration buried layerWhile forming the reversal region of a low electric field in the direction of channel length on said high concentration buried layer which impressed operating voltage to said drain diffusion region and said gate electrodeand said optical generating electron hole accumulatedA high electric field field is formed in the channel regions except said high concentration buried layer top in said direction of channel lengthThe operating voltage that said insulated gate field effect transistor operates by saturation to said drain diffusion region and

said gate electrode is impressedBy having formed said insulated gate field effect transistor in the source followerand having accumulated said optical generating electron hole in said high concentration buried layerchange of the threshold voltage of said insulated gate field effect transistorIt is characterized by detecting a signal by changing into the electrical change of the source diffusion area of said insulated gate field effect transistor.

[0023]In a lightwave signal detecting method invention of Claim 14 relates to a lightwave signal detecting method by a solid state image pickup deviceand according to the solid state image pickup device according to any one of claims 1 to 10Said semiconductor substratesaid well areaand said high concentration buried layer are n typesSaid semiconductor layersaid impurity diffusion regionsaid drain diffusion regionand said source diffusion area are p typesLarger voltage to a negative side than operating voltage is impressed to said impurity diffusion regionsaid drain diffusion regionsaid gate electrodeand said source diffusion areaTo said semiconductor layeran electron hole for an electron in said well area and a high concentration buried layer Said impurity diffusion regionA pixel is initialized by discharging to said drain diffusion region and said source diffusion arearespectivelyand depletion-izing to themAn electron hole and an electron are produced in a well area of said euphotic diode by optical exposureOperating voltage is impressed to said impurity diffusion region and said drain diffusion regionAnd a potential twist of said euphotic diode also impresses voltage which becomes high to said gate electrodepotential of a gate region of said insulated gate field effect transistor moves inside of said well area for said optical generating electron to itand said optical generating electron is stored up in said high concentration buried layerWhile forming a reversal region of a low electric field on said high concentration buried layer which impressed operating voltage to said drain diffusion region and said gate electrodeand said optical generating electron accumulatedForm a high electric field field in channel regions except said high concentration buried layer topand operating voltage that said insulated gate field effect transistor operates by saturation to said drain diffusion region and said gate electrode is impressedChange of threshold voltage of said insulated gate field effect transistor by having formed said insulated gate field effect transistor in a source followerand said optical

generating electron having been accumulated in said high concentration buried layerIt is characterized by detecting a signal by changing into an electrical change of a source diffusion area of said insulated gate field effect transistor.

[0024]In this inventionare in a well area under channel regionsand near a source diffusion areaFor exampleit is a partial area of the direction of channel length from a drain diffusion region to a source diffusion areathe source diffusion area side -- and a part of cross direction of channel regions -- or it crossed crosswise [whole] and a high concentration buried layer (carrier pocket) which has the one same conductivity type as a well areaand has impurity concentration higher than a well area is provided.

[0025]For examplewhen using a gate electrode of ring shapea source diffusion area is formed in a surface of a well area of a center section of the gate electrodea drain diffusion region is formed in a surface of a well area so that a gate electrode may be surroundedand a high concentration buried layer is formed in a well area so that a source diffusion area may be surrounded. In the case of a p type high concentration buried layer in a p type well areain such compositionpotential becomes the lowest to an electron hole in a place of a p type high concentration buried layer. Or in the case of a n type high concentration buried layer in a n type well areapotential becomes the highest to an electron in a place of a n type high concentration buried layer.

[0026]A well area is formed in common by euphotic diode and a field effect transistor in [an impurity diffusion region of a euphotic diodeand a drain diffusion region of a field effect transistor] one. A high concentration buried layer is provided near the source diffusion area. Since a high concentration buried layer is arranged near the source diffusion areait is easy to bring an optical generating electric charge generated in a well area of a euphotic diode section in a high concentration buried layer together.

[0027]That iswhen a detecting transistor is set to nMOSusing a p type well areathe potential in the direction of a source diffusion area is low set up rather than a drain diffusion region using an electron hole among optical generating electric charges. Or when a detecting transistor is set to pMOSusing a n type well areathe potential in the direction of a source diffusion area is highly set up rather than a drain diffusion region using an electron among optical generating electric charges. For examplewhen the positive or negative operating voltage VDD is impressed

to a drain diffusion region and low voltage is impressed to a gate electrodethe electric field that an optical generating electric charge goes to the direction of a source diffusion area from the drain diffusion region of a field effect transistori.e.the impurity diffusion region of a euphotic diodearise.

[0028]Thereforewhen voltage is impressed as mentioned above after discharging residual chargesuch as an electron hole which carbonates the optical generating electric charge which read-out finishedthe acceptor in a well areaetc. by initializationout of a semiconductor substrateThe optical generating electric charge generated in the well area of a euphotic diode section moves to the direction of a high concentration buried layerand is accumulated in a high concentration buried layer. Since it is the low potential there and it becomes impossible to escape easily once optical generating electric charges gather for a high concentration buried layerdiffusion of the optical generating electric charge in a well area can be preventedand an optical generating electric charge can be efficiently accumulated in a high concentration buried layer.

[0029]It can eliminate by impressing larger voltage than operating voltage to a gate electrodea drain diffusion regionand a source diffusion areaand raising electric field also by the optical generating electric charge accumulated in the high concentration buried layer. If an optical generating electric charge is accumulated into a high concentration buried layera Fermi level changes according to an accumulated doseand space charge will bring about the fall of the threshold voltage of a transistor in order to decrease in number. Simultaneouslywith conservation of chargea reversal region is formed on a high concentration buried layerthe carrier of a conductivity type contrary to the optical generating electric charge accumulated into the high concentration buried layer in the reversal region increasesand channel conductance increases.

[0030]On the other handsince potential is high in fields other than a high concentration buried layer and an optical generating electric charge is not accumulateda reversal region will not be generated in the well area surfaces other than on a high concentration buried layerbut a high electric field field will produce. Thuswhen a reversal region and a high electric field field produce in one channel regionsthe transistor comes to operate by saturation. Thereforeif the gate voltage in which the transistor can operate is impressed to gate voltagethe

transistor by which wiring connection was made as a source follower will follow in footsteps of threshold voltageand will change source potential.

[0031]And since the transistor operates by saturationcurrent is decided only by potential difference between gate sources. For this reasonchange of source potential is decided only by the accumulated dose of an optical generating electric charge. Thereforeit becomes possible by outputting this source potential as a video signal to perform photoelectric conversion with sufficient linearity.

[0032]Since a fluctuated part of an accumulated dose of an optical generating electric charge and an electric charge of a reversal region is balancedan accumulated dose of an optical generating electric charge is equivalent to a charge to gate-dielectric-film capacityand a changed part of threshold voltage is outputted. Heresince charge to gate-dielectric-film capacity is limited to gate-dielectric-film capacity on a high concentration buried layer as a carrier pocketit can determine detection sensitivity with area and the depth of oxide film thicknesses and a high concentration buried layer. And since it can consider that most of this detecting capacity is fixed capacityhigh sensitivity detection which was extremely excellent in the linearity of the transfer characteristic of electric charge-voltage conversion is attained.

[0033]When the surface of a transistor has DEPURESHON-izeda barrier will exist to a hole. Since the surface is filled with photogate electrode structure used by other systems by an optical generating electric charge at this timethe surface is equilibrated and dark current generating by thermal excitation and potential abnormal conditions by a parasitism hole storage pose a problem.

[0034]On the other handin this inventionchannel regions of a transistor sweep out residual charge (initialization)and a depletion state is held behind. And since a transistor region is shadedit does not come to form a superfluous carrier layer. Thereforea carrier temporarily captured on the surface is also made not to overcome a barrierit does not become dark currentand a noise component can be controlled from the surface.

[0035]As mentioned above********** pouring of the optical generating electric charge which should control current is carried out under the isolated channel regions which interact with neither of the semiconductor layer surface portionsand the potential barrier near a source diffusion

area is changed. That isby collecting optical generating electric charges near the source diffusion areaby considering it as structure which controls the threshold voltage of a transistorit cannot have a noise component but the ideal threshold voltage modulation method CMOS image sensor element in which high sensitivity detection is possible can be provided with sufficient linearity.

[0036]

[Embodiment of the Invention]Belowan embodiment of the invention is describedreferring to Drawings. Drawing 1 is a top view showing the element layout in the unit pixel of the CMOS image sensor concerning an embodiment of the invention. As shown in drawing 1the euphotic diode 111 and MOS transistor 112 for lightwave signal detection are adjoined and formed in the unit pixel 101. These are sharing the one well area 15. That isthe well area 15 of the euphotic diode 111 constitutes the generating region of the electric charge by optical exposureand the well area 15 of MOS transistor 112 for lightwave signal detection constitutes the gate region.

[0037]The impurity diffusion region 17 of the euphotic diode 111 and the drain diffusion region 17a of MOS transistor 112 for lightwave signal detection are formed in the surface of the well area 15 in one. The drain diffusion region 17a is formed so that the outer peripheral part of the gate electrode 19 of ring shape may be surroundedand the source diffusion area 16 is formed in the central part of the gate electrode 19 of ring shape. It is in the well area 15 under the gate electrode 19and the carrier pocket (high concentration buried layer) 25 is formed so that the source diffusion area 16 may be surrounded in the periphery of the source diffusion area 16.

[0038]The n type impurity layer (opposite conductivity type impurity layer) which introduced the n type impurity is formed in channel regions so that the channel regions of the surface of the well area 15 under the gate electrode 19 may maintain an inverted state or a DEPURESHON state at the time of operation of MOS transistor 112 for lightwave signal detection. The drain diffusion region 17a is connected with the drain voltage (VDD) supply line 22the gate electrode 19 is connected to the vertical-scanning-signals (VSCAN) supply line 21and the source diffusion area 16 is connected to the vertical output line 20.

[0039]Fields other than sensor window 24 of the euphotic diode 111 are shaded by the metal layer (light-shielding film) 23. Nextthe device structure of the CMOS image sensor concerning an embodiment of the invention is explained

using a sectional view. The figure on drawing 2 is a sectional view showing the device structure of the CMOS image sensor concerning an embodiment of the invention equivalent to the A-A line sectional view of drawing 1. The figure under drawing 2 is a potential figure along a semiconductor substrate surface.

[0040]The figure on drawing 3 is a sectional view showing near the carrier pocket 25 in the well area 15 under channel regions in detail. The figure under drawing 3 is a potential figure which meets the F-F line in a field parallel to the semiconductor substrate surface containing the carrier pocket 25 when the optical generating hole is accumulated in the carrier pocket 25i.e.a figure. Howeverdistribution of the electron of the reversal region of the channel regions on the carrier pocket 25 is indicated to the same figure.

[0041]Drawing 4 is a B-B line sectional view of drawing 1and drawing 5 is a C-C line sectional view of drawing 1. As shown in the figure on drawing 2on the substrate 11 which consists of p type siliconn type silicon is grown epitaxially and the epitaxial layer (n type layer) 12 is formed. The above constitutes a semiconductor substrate. The p type well region 15 is formed in this n type layer 12. The field insulating films 14 and the isolation diffusion region 13 under it are formed so that each unit pixel may be separated between the adjoining unit pixels.

[0042]Nextdrawing 2 and drawing 4 explain the details of the euphotic diode 111. That isit comprises the well region 15 and the impurity diffusion region 17 formed in the surface of the n type layer 12 so that most fields might start the well region 15. That isit is having the embedded structure to an electron hole (hole). It is connected to the drain voltage (VDD) supply line 22and bias of the impurity diffusion region 17 is carried out to electropositive potential. Therebyin order for the hole generated by incident light to exist in the well region 15 under the impurity diffusion region 17it is not influenced in a semiconductor layer surface with many interface trapping levelsbut can aim at reduction of noise.

[0043]Nextdrawing 2 and drawing 5 explain the details of MOS transistor (nMOS) 112 for lightwave signal detection. That isit has the structure where the gate electrode 19 of ring shape was surrounded by the n^+ type impurity diffusion region 17 and the n^+ type drain diffusion region 17a formed in one. The n^+ type source diffusion area 16 is formed in the center section of the gate electrode 19 of ring shape. And the gate electrode 19 is formed via the gate dielectric

film 18 on the well area 15 between the drain diffusion region 17a and the source diffusion area 16. The surface of the well area 15 under the gate electrode 19 serves as channel regions.

[0044]In the well area 15 under channel regionsit is a periphery of the partial area 16 of the direction of channel lengthi.e.a source diffusion areaand the p^+ type carrier pocket 25 is formed so that the source diffusion area 16 may be surrounded. This p^+ type carrier pocket 25 can be formedfor example with ion implantation. The carrier pocket 25 is formed in the well area 15 below the channel regions produced on the surface. As for the carrier pocket 25forming so that channel regions may not be started is desirable. In normal operation voltagein order to hold channel regions in an inverted state or the DEPURESHON stateit is required to introduce the n type impurity of the suitable concentration for channel regionsand to form the n type impurity layer 15a.

[0045]In the above-mentioned p^+ type carrier pocket 25since the potential over an optical generating hole becomes low among optical generating electric chargeswhen high tension is impressed to the drain diffusion region 17aoptical generating holes gather for this carrier pocket 25. A figure shows the state where the optical generating hole is accumulated in the carrier pocket 25. An optical generating hole is accumulated in the following figure of drawing 2 at the carrier pocket 25and the potential figure in the state where the electron was induced by channel regions and the reversal region has produced is shown. The element structure section near the carrier pocket 25 in the well area 15 under channel regions and the details of a potential figure are shown in drawing 3.

[0046]Nextwith reference to drawing 6 (a) and (b)the composition of the whole CMOS image sensor using the unit pixel of the above-mentioned structure is explained. Drawing 6 (a) shows the circuitry figure of the CMOS image sensor in an embodiment of the invention. As shown in drawing 6 (a)this CMOS image sensor has taken the composition of the two-dimensional array sensorand it is arranged so that the unit pixel of the above-mentioned structure may be located in a line with matrix form at a line direction and a line writing direction.

[0047]The drive scanning circuit 102 of vertical scanning signals (VSCAN) and the drive scanning circuit 103 of drain voltage (VDD) are arranged across the picture element region at the right and left. the drain voltage supply lines 22a and 22b which have come out from the drive

scanning circuit 103 of drain voltage (VDD) are connected to every one drain per line of MOS transistor 112 in all the unit pixels 101 located in a line with a line writing direction for every linerespectively. the vertical-scanning-signals supply lines 21a and 21b which have come out from the drive scanning circuit 102 of vertical scanning signals (VSCAN) to every one gate per line of MOS transistor 112 in all the unit pixels 101 located in a line with a line writing direction for every line are connectedrespectively.

[0048]The source of MOS transistor 112 in all the unit pixels 101 located in a line with a line direction for every sequence is connected to the different vertical output lines 20a and 20b for every sequence. Each vertical output lines 20a and 20b are connected to every one drains (photodetection signal input terminal) 28a and 29a of MOS transistors 105a and 105b as a different switch for every sequence. The gates (horizontal scanning signal input terminal) 28b and 29b of each switches 105a and 105b are connected to the drive scanning circuit 104 of a horizontal scanning signal (HSCAN).

[0049]The sources (photodetection signal output terminal) 28c and 29c of each switches 105a and 105b are connected to the video signal outputs 107 through the common constant current source 106. That isit is connected to the constant current source 106and the source of MOS transistor 112 in each unit pixel 101 forms the source follower circuit of a pixel unit. Thereforethe potential difference between the gate sources of each MOS transistor 112 and the potential difference between bulk sources are determined by the connected constant current source (load circuit) 106.

[0050]The video signal (Vout) which drove MOS transistor 112 of sequential ** each unit pixeland is proportional to the amount of incidence of light with vertical scanning signals (VSCAN) and a horizontal scanning signal (HSCAN) is read. As mentioned abovesince the unit pixel 101 comprises the euphotic diode 111 and MOS transistor 112the portion of a pixel can be created using a CMOS technology. Thereforeall of the above-mentioned picture element partand the drive scanning circuits 102-104 and a constant current source 106 grade peripheral circuit can be created to the same semiconductor substrate.

[0051]Drawing 6 (b) shows the timing chart of each input output signal for operating the CMOS image sensor concerning this invention. Using the p type well area 15when the transistor 112 for lightwave signal detection is nMOSit applies. Element operation is a **** period

(initialization)-storage period-read-out period-**** period (initialization). - It carries out repeatedly like ..
[0052]At this timesigns that the potential in the well area 15 of the unit pixel 101 changes with operation of a solid state image pickup device are also explained simultaneouslyreferring to drawing 7drawing 8and the potential figure of drawing 9. It explains simultaneouslyreferring to the graph shown in drawing 10 about the current/voltage characteristics of MOS transistor 112 for lightwave signal detection in the unit pixel 101.
[0053]In drawing 7 thru/or drawing 9a vertical axis expresses potential and a horizontal axis expresses the depth from a substrate face. Drawing 7 (a)drawing 8 (a)and drawing 9 (a) express the potential distribution in the D-D line section of drawing 4 in a **** period (initialization)a storage periodand a read-out periodrespectively. Drawing 7 (b)drawing 8 (b)and drawing 9 (b) express the potential distribution in the E-E line section of drawing 5 in a **** period (initialization)a storage periodand a read-out periodrespectively.
[0054]Firsta **** period is a period which discharges residual charge before read-out of a lightwave signalsuch as an electron holean electronetc. which carbonate an optical generating electric chargean acceptora donoretc. whom read-out finishedor are captured by the surface levelout of a semiconductorbefore accumulating an optical generating electric charge (hole). That isthis operation is called substrate **** operation (initializing operation) of an optical generating electric chargeand it is carried out per line.
[0055]Initializing operation is performed in order to make the carrier pocket 25 the next storage period in the sky and to accumulate a new optical generating electric charge. That isit is for taking out only the accumulated optical generating electric charge as a video signaland preventing the noise by residual charge. In this caselarger voltage than the usual operating voltage is impressed to the drain diffusion region 17athe gate electrode 19and the source diffusion area 16. That isthe voltage of abbreviation+5V is supplied to the VDD supply lines 22a and 22bit is impressed by the drain diffusion region 17athe voltage of abbreviation+5V is supplied to the VSCAN supply lines 21a and 21band it is impressed by the gate electrode 19. Since channel regions conduct by impressing the voltage of abbreviation+5V to the gate electrode 19the voltage of abbreviation+5V impressed to the drain diffusion region 17a is impressed to the source diffusion area 16 as it is.

[0056]This voltage impressing carries out reverse bias of the pn junctionas shown in drawing 7 (a) and (b)and it is made suitable [the electric field in the well region 15] in the substrate 11 direction of a p^+ type through N field and P field. The hole which remains in well area 15 and other semiconductors is discharged by the p^+ type substrate 11 by thisand an electron is discharged from the source diffusion area 16 or the drain diffusion region 17. When the optical generating electric charge is especially accumulated in the carrier pocket 25a transistor cannot make an optical generating electric charge discharge from the carrier pocket 25 in the gate voltage and drain voltage which can operate by saturationbut. An optical generating electric charge can be made to discharge from the carrier pocket 25 by impressing still higher gate voltage and drain voltage of about [5V].

[0057]After residual charge is dischargedthe well area 15 is in the state where it depletion-ized. Since initialization which was described above does not produce residual chargethe thermal noise (kTC noise) by the thermal fluctuation of a carrier does not occurbut it is ideal. In this initializing operationsince there is no current paththe booster circuit carried on chip can use it easily.

[0058]Nexta storage period is a period which generates an optical generating electric charge by optical exposureand stores up the optical generating electric charge in the carrier pocket 25 in the well area 15 under channel regions. In this storage periodthe electronic shutter operation in a horizontal scanning time basis is also possible. In this casewhile impressing the voltage which lets the VDD supply lines 22a and 22b passto which the MOS transistor can operate before an optical exposure to the drain diffusion region 17 of MOS transistor 112 in all the unit pixels 101 and which is about +2-3V aboutIt lets the VSCAN supply lines 21a and 21b passand the low voltage that a MOS transistor maintains a cutoff state to the gate of MOS transistor 112 for every sequence is impressed. Thusaccumulation of an optical generating electric charge is performed for every sensor column arranged on each horizontal scanning signal line.

[0059]Since the majority carrier (electron hole) in the p type well region 15 is swept out by the voltage impressing to the drain diffusion region 17a at the p^+ board 11 side of typethe inside of the well region 15 is depletion-izedand the negative space charge layer which consists of acceptors exists by it. If a picture element region is irradiated in this statean electronic-electron hole pair will occur in

the well area 15 of the euphotic diode 111.
[0060]Heresince the gate voltage of MOS transistor 112 is set up lowan optical generating electron is discharged by drain voltage from the drain diffusion region 17 among optical generating electric charges. On the other handit is pulled to the low potential of the source diffusion area 16and moves to the direction of the source diffusion area 16and an optical generating hole is accumulated in the carrier pocket 25 which is the lowest [potential]. This state is shown in drawing 8 (a) and (b).
[0061]Since movement of the optical generating hole in a storage period is performed only in the p type well area 15on the occasion of movement of an optical generating holeit is not influenced by a semiconductor surfaceand a noise component is not generated. By the waywhen the surface of a transistor has DEPURESHON-izeda barrier will exist to a hole.
[0062]Since the surface is filled with the photogate electrode structure used by other systems by the optical generating electric charge as shown in drawing 11 (c)the surface is equilibrated and dark current generating by thermal excitation and the potential abnormal conditions by a parasitism hole storage pose a problem. On the other handin this embodimentas the channel regions of a transistor are shown in drawing 11 (a)a depletion state is held after initialization. And since the gate of a transistor and its circumference are shaded as shown in drawing 11 (b)it does not come to form a superfluous carrier layer. Thereforethe carrier temporarily captured on the surface is also made not to overcome a barrierit does not become dark currentand the noise component from the surface can be controlled.
[0063]A read-out period is a period which reads the video signal (Vout) based on the accumulated optical generating electric charge. MOS transistor 112 for lightwave signal detection is operated as a source follower circuitand a video signal (Vout) is outputted. In this casewith the VDD supply lines 22a and 22bwhile impressing about [+2-3V] voltage to the drain of MOS transistor 112 about for every lineso that MOS transistor 112 may operate by saturationAbout [+2-3V] voltage is about impressed to the gate of MOS transistor 112 for every sequence with the VSCAN supply lines 21a and 21b. The constant current source 106 is connected to the source of MOS transistor 112 for lightwave signal detectionand fixed current is sent.
[0064]By the waythe optical generating electric charge is accumulated into the carrier pocket 25 in the storage

period in front of this read-out period. If an optical generating electric charge is accumulated into the carrier pocket 25a Fermi level changes according to an accumulated doseand space charge will bring about the fall of the threshold voltage of a transistor in order to decrease in number. Simultaneouslywith conservation of chargea reversal region is formed on the carrier pocket 25the electron of the same quantity as the quantity of the optical generating hole accumulated into the carrier pocket 25 in the reversal region increasesand channel conductance increases.

[0065]In this casethe surface potential on the carrier pocket 25 serves as about 1 constant value in a gate length directionand the electron which is a carrier is distributed over a reversal region by uniform density. On the other handin the drain diffusion region 17a sidesince space charge density is lowit is not generated on the surface but a high electric field field produces a reversal region on it. Thussince the reversal region produced in some channel regions and the high electric field field has produced into other portionsas shown in drawing 10operation of MOS transistor 112 for lightwave signal detection by saturation is attained.

[0066]Thereforeif the usual operating voltage is impressed to each electrode of MOS transistor 112 for lightwave signal detectionthe transistor 112 will operate by saturation. Since the transistor 112 forms the source follower circuit by constant current operation at this timeas shown in drawing 9 (a) and (b)source potential becomes highin order to decrease the potential difference between gate sources so that constant current may flow into the transistor 112 by a negative feedback operation. Change of this source potential is outputted to the video signal outputs 107.

[0067]He may understand the above-mentioned reading operation as follows. That isas shown in drawing 10in order that MOS transistor 112 for lightwave signal detection may operate in a saturation regionthe potential difference between drain sources is determined by the potential under the gate electrode 19and the electric field of source diffusion area 16 direction exist in the p type well region 15 according to the potential difference.

[0068]Thereforealthough an optical generating hole changes the Fermi potential of the source diffusion area 16 neighborhood to a positive directionsince the current value is determined by the constant current source 106the potential barrier height by the side of a source is saved. For this reasonas shown in drawing 9 (a) and (b)in source

potential (VS)change for the potential difference of the space charge layer carbonated by pouring of the optical generating hole appears. That isbulk potential can be changed with the amount of optical generating holesand a source follower output can be changed.
[0069]Therebythe video signal (Vout) proportional to an optical dose can be obtained. In this casesince a fluctuated part of the electric charge of an optical generating hole and a reversal region is balancedthe charge quantity by an optical generating hole is equivalent to the charge to gate-dielectric-film 18 capacityand a changed part of threshold voltage is outputted. Hereas shown in drawing 12 (a) and (b)since the charge to gate-dielectric-film 18 capacity is limited to gate-dielectric-film 18 capacity on the carrier pocket 25it can determine detection sensitivity with the area and the depth of gate oxide thickness and the carrier pocket 25. Since an optical generating hole is accumulated in a limited field called the carrier pocket 25conversion efficiency is also good.
[0070]And since it can consider that most of this detecting capacity is fixed capacitythe high sensitivity detection which was extremely excellent in the linearity of the transfer characteristic of electric charge-voltage conversion is attained. Nextaccording to drawing 6 (a) and (b)photodetection operation of a series of continuous solid state image pickup devices is explained briefly. That isthe electric charge which remains in the semiconductor layer of a well area or others by initializing operation is discharged.
[0071]Subsequentlylow gate voltage is impressed to the gate electrode 19 of a transistorand the voltage (VDD) of about two to 3 V required for operation of a transistor is impressed to the drain diffusion region 17a. At this timethe well area 15 is depletion-ized and the electric field which go to the source diffusion area 16 produce it from the drain diffusion region 17a. If an electronic-hole pair (optical generating electric charge) arises by optical exposurean optical generating hole will be poured into a gate region among this optical generating electric charge by the above-mentioned electric fieldand it will be accumulated in the carrier pocket 25. While the depletion layer width which spreads in the substrate 11 side from channel regions is restricted by thisthe potential of the source diffusion area 16 neighborhood is modulatedand the threshold voltage of MOS transistor 112 is changed.
[0072]HereMOS transistor 112 impresses the gate voltage of about two to 3 V which can operate by saturation to the

gate electrode 19and the voltage VDD which is about 2-3V to which MOS transistor 112 can operate to the drain diffusion region 17a is impressed. Therebythe reversal region of a low electric field is formed in some channel regionsand a high electric field field is formed in the remaining portion.

[0073]The constant current source 106 is connected to the source diffusion area 16 of MOS transistor 112and fixed current is sent. Therebya source follower circuit is formedtherefore it follows in footsteps of change of the threshold voltage of the MOS transistor by an optical generating holesource potential changesand MOS transistor 112 brings about change of output voltage. Therebythe video signal (Vout) proportional to an optical dose can be taken out.

[0074]As mentioned aboveaccording to this embodiment of the inventionin a series of processes of ******** (initialization)-accumulation operation-reading operationwhen an optical generating hole movesthe ideal photoelectric conversion mechanism which does not interact with the noise source in a semiconductor surface or channel regions can be realized. Since the carrier pocket 25 is formed in the partial area under channel regionssome channel regions can be made into a reversal regionand the remaining portion can be made into a high electric field field. Therebyas shown in drawing 10a transistor can be operated by saturation. And since the source follower circuit is formedchange of the threshold voltage by an optical generating electric charge is detectable as change of source potential. For this reasonphotoelectric conversion with sufficient linearity can be performed.

[0075]In the case of the BCMD type solid state image pickup device of the conventional example shown in drawing 13 (b)current/voltage characteristics turn into the triode characteristic and operation by saturation is difficult for them. For this reasonit can be said that it is difficult to perform photoelectric conversion with sufficient linearity. Since the euphotic diode 111 and MOS transistor 112 for lightwave signal detection are formed independentlydegradation of the spectral sensitivity characteristic by multiple interference like the optical exposure to a photogate electrode can be prevented.

[0076]Since element composition can be performed in the simple combination of the euphotic diode 111 and MOS transistor 112 for lightwave signal detectionit can improve a numerical aperture. Gate voltage can be changed and fixed pattern noise can be controlled taking advantage of the

characteristic that the gain and source capacity of a source follower can be adjusted. Although the p+ type carrier pocket 25 was formed in the p type well area 15the hole was accumulated and the nMOS transistor (MOS transistor for lightwave signal detection) 112 has detected the lightwave signal in the above-mentioned embodimentUsing a n type well areaan n+ type carrier pocket is providedan electron is accumulatedand it may be made for a pMOS transistor (MOS transistor for lightwave signal detection) to detect a lightwave signal.

[0077]He is trying to impress the voltage of abbreviation+5V which made carry out conduction of the channel regionsand was impressed to the drain diffusion region 17a to the source diffusion area 16 as it is in drawing 6 (a) in which the composition of the whole solid state image pickup device is shown by impressing the voltage of abbreviation+5V to the gate electrode 19 in a **** period. Howevera power supply with which only a **** period supplies the voltage of abbreviation+5V to the source diffusion area 16 via a switching means may be independently connected to the source diffusion area 16.

[0078]In drawing 6 (a) in which the composition of the above-mentioned whole solid state image pickup device is shownalthough the constant current source is used as a load circuitvolume load may be used. In this casesince capacity will be charged by that change if the source potential of the transistor 112 for lightwave signal detection changes with accumulation of an optical generating electric chargethose charge voltages can be taken out as a video signal. It is possible to use the load circuit of others which have high impedance which forms a source follower other than a constant current source or volume load.

[0079]

[Effect of the Invention]As mentioned abovein the solid state image pickup device of the threshold voltage modulation method concerning this inventionIt had the euphotic diode and insulated gate field effect transistor which share a well areaand has the high concentration buried layer (carrier pocket) near the source diffusion area in the well area under the channel regions of a transistor.

[0080]For this reasonthe inside of a semiconductor can be movedthe optical generating electric charge generated in the euphotic diode part can be stored up in a high concentration buried layerand the threshold voltage of a transistor can be changed. Thereforethermal noise (kTC noise)semiconductor surface capture noiseetc. can be

controlled until it results in **** (initialization) of residual chargephotoelectric conversionaccumulationand voltage conversion. Therebythe solid state image pickup device of low noise can be providedand the performance of an MOS type image sensor can be improved beyond the performance of a CCD type image sensor.

[0081]Since the high concentration buried layer is provided in the partial area under channel regionssome channel regions can be made into a reversal regionand the remaining portion can be made into a high electric field field. Therebya transistor can be operated by saturation. And since the source follower circuit which connected the load circuit of the high impedance represented with a constant current drive is formedchange of the threshold voltage by an optical generating electric charge is detectable as change of source potential. For this reasonphotoelectric conversion with sufficient linearity can be performed.

[0082]Since element composition can be performed in the simple combination of a euphotic diode and the MOS transistor for lightwave signal detectionit can improve a numerical aperture. Gate voltage can be changed and fixed pattern noise can be controlled taking advantage of the characteristic that the gain and source capacity of a source follower can be adjusted. By the existing CMOS process technologysince manufacture of a light sensing portion is possiblea peripheral circuit can also be created to the same substrate very inexpensive.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a top view showing the element layout in the unit pixel of the solid state image pickup device concerning an embodiment of the invention.

[Drawing 2]It is an A-A line sectional view of drawing 1 showing the structure of the element in the unit pixel of the solid state image pickup device concerning an embodiment of the invention.

[Drawing 3]It is a sectional view showing the carrier pocket in the unit pixel of the solid state image pickup device concerning an embodiment of the inventionand the details of the periphery.

[Drawing 4]It is a B-B line sectional view of drawing 1 showing the structure of the euphotic diode in the unit pixel of the solid state image pickup device concerning an embodiment of the invention.

[Drawing 5]It is a C-C line sectional view of drawing 1 showing the structure of the MOS transistor for lightwave signal detection in the unit pixel of the solid state image pickup device concerning an embodiment of the invention.
[Drawing 6]Drawing 6 (a) is a figure showing the circuitry of the whole solid state image pickup device concerning an embodiment of the invention. Drawing 6 (b) is a timing chart at the time of operating the solid state image pickup device of drawing 6 (a).
[Drawing 7]Drawing 7 (a) is a figure in the state where there is a **** period at the time of operation of the solid state image pickup device concerning an embodiment of the invention showing the potential distribution in the D-D line section of drawing 4. Drawing 7 (b) is a figure in the state where there is a **** period at the time of operation of the solid state image pickup device concerning an embodiment of the invention showing the potential distribution in the E-E line section of drawing 5.
[Drawing 8]Drawing 8 (a) is a figure in the state where there is a storage period at the time of operation of the solid state image pickup device concerning an embodiment of the invention showing the potential distribution in the D-D line section of drawing 4. Drawing 8 (b) is a figure in the state where there is a storage period at the time of operation of the solid state image pickup device concerning an embodiment of the invention showing the potential distribution in the E-E line section of drawing 5.
[Drawing 9]Drawing 9 (a) is a figure in the state where there is a read-out period at the time of operation of the solid state image pickup device concerning an embodiment of the invention showing the potential distribution in the D-D line section of drawing 4. Drawing 9 (b) is a figure in the state where there is a read-out period at the time of operation of the solid state image pickup device concerning an embodiment of the invention showing the potential distribution in the E-E line section of drawing 5.
[Drawing 10]It is a graph which shows the current/voltage characteristics of the MOS transistor for lightwave signal detection in the unit pixel of the solid state image pickup device concerning an embodiment of the invention.
[Drawing 11]Drawing 11 (a) is a figure showing the state on the surface of a channel layer after electric charge reset of a solid state image pickup device.
Drawing 11 (b) is a figure showing the state on the surface of a channel layer of the solid state image pickup device concerning an embodiment of the inventionand drawing 11 (c) is a figure showing the state on the surface of a channel

layer of the solid state image pickup device of the photogate structure concerning a conventional example.

[Drawing 12]Drawing 12 (a) is a figure showing the distribution state of the electric charge from the storage period to a read-out period at the time of operation of the solid state image pickup device concerning an embodiment of the invention. Drawing 12 (b) is a carrier pocket for explaining drawing 12 (a)and an element sectional view of the neighborhood.
[Drawing 13]Drawing 13 (a) is a sectional view showing the structure of the solid state image pickup device of the BCMD structure concerning a conventional example. Drawing 13 (b) is a graph which shows the current/voltage characteristics of the solid state image pickup device of the BCMD structure concerning a conventional example.
[Explanations of letters or numerals]
15 Well area
15a N type impurity layer (opposite conductivity type impurity layer)
16 and 16a source diffusion area
17 Impurity diffusion region
17a Drain diffusion region
19 Gate electrode
2020aand 20b Vertical output line
2121aand 21b A vertical-scanning-signals (VSCAN) supply line
2222a22b drain voltage (VDD) supply line
25 A carrier pocket (high concentration buried layer)
26 A level output line
27a and 27b A horizontal scanning signal (HSCAN) supply line
28a and 29a A photodetection signal input terminal
28b and 29b A horizontal scanning signal input terminal
28c and 29c A photodetection signal output terminal
101 A unit pixel
102 A vertical-scanning-signals (VSCAN) drive scanning circuit
103 A drain voltage (VDD) drive scanning circuit
104 A horizontal scanning signal (HSCAN) drive scanning circuit
105a and 105b A switch
106 A constant current source (load circuit)
111 A euphotic diode
112112a A MOS transistor for lightwave signal detection.